REMARKS

Applicant appreciates Examiner Mais' time and attention associated with the telephonic interview with the undersigned on June 11, 2009. The discussion related to proposed claim amendments to claims 1, 23, 37 and 51, and potential distinctions over Baker, *et al.* (U.S. Patent Number 5,983,301). Applicant appreciates Examiner Mais' consideration of the present Amendment.

Claims 1-4, 8-54 and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Baker, *et al.* (U.S. Patent Number 5,983,301). Claims 5-7 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-22, a system for transferring a signal to a channel includes a storage unit dedicated to the channel for storing source identification information of a plurality of predetermined sources. The source identification information indicates an order of priority of the plurality of predetermined sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the storage unit, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

Claims 1-22 are amended to clarify that the plurality of selection circuits receive input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the storage unit. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 23-36, a system for transferring signals to channels includes a plurality of storage units, each storage unit being dedicated to one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of a plurality of predetermined sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the plurality of storage units, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

Claims 23-36 are amended to clarify that the plurality of selection circuits receive input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the plurality of storage units. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 37-50, a direct memory access (DMA) controller for controlling transfer of signals from predetermined input sources to output devices, a plurality of channels being connected to the output devices, includes a plurality of storage units, each storage unit being dedicated to one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the predetermined sources for access to the channel. The system further includes a plurality of selection circuits for receiving input signals from at least one of the predetermined sources and the source identification information of the predetermined sources from the plurality of storage units, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The system further includes a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel.

Claims 37-50 are amended to clarify that the plurality of selection circuits receive input signals from at least one of the predetermined sources and the source identification information of the predetermined sources from the plurality of storage units. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 51-72, a method of transferring a signal to a channel includes storing source identification information for a plurality of predetermined sources. The source identification information indicates an order of priority of the plurality of predetermined sources for access to the channel. The method further includes providing a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information. The method further includes, with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel.

Claims 51-72 are amended to clarify that the plurality of selection circuits receive input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Baker, *et al.* discloses, as illustrated in FIG. 4 of Baker, *et al.*, that receive data 106 includes header data 108 having words WD0 and WD1. Words WD0 and WD1 of the receive data 106 are provided to each of the N DMA channel header compare blocks 110. DMA header compare registers for each DMA channel in logic 110 includes a WD 0 field select register 122, a WD 1 select register 126, a WD 0 compare value register 120 and a WD 1 compare value register 124. The two field select registers 122 and 126 specify the bit fields in WD0 and WD1 of the incoming packet 106 that will be matched to an expected value by the comparator logic. The two compare value registers 120 and 124 specify the expected bit patterns that will be matched against the selected bit fields in

WD0 and WD1 of the incoming packet 106. An output of DMA header compare registers and logic 110 is represented as channel select [0] through channel select [N-1]. As illustrated in FIG. 4 of Baker, *et al.*, the priority encoder 128 receives these channel select outputs to produce and provide a channel number at DMA channel selected line 130 and an address match output 132 to IEEE 1394 receiver logic 102. The Baker, *et al.* DMA header compare registers and logic 110 and priority encoder 128 implement the logic required to determine if an incoming packet is to be accepted and loaded into the GRF 80. The IEEE 1394 receiver logic 102 uses the DMA channel number, and comparator match indication to determine if the incoming packet is to be received into the GRF 80. In Baker, *et al.*, the header information 108 from the received data 106 is used to determine the channel number of the incoming packet.

Baker, *et al.* fails to teach or suggest a system for transferring a signal to a channel which includes a storage unit dedicated to the channel for storing source identification information of a plurality of predetermined sources, and a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the storage unit, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information which indicates an order of priority of the plurality of predetermined sources for access to the channel, as claimed in claims 1-22. In addition, Baker, *et al.* fails to teach or suggest a system for transferring signals to channels includes a plurality of storage units, each storage unit being dedicated to one of the channels, and each storage unit being adapted to store source identification information indicating an order of priority of the plurality of predetermined sources for access to the channel, and a plurality of selection circuits, for each or the plurality of channels, for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources from the plurality of storage units, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information, as claimed in claims 23-36. Further, Baker, *et al.* fails to teach or suggest a direct memory access (DMA) controller that includes a plurality of storage units, each storage unit being dedicated to one of the channels, and each storage unit

being adapted to store source identification information indicating an order of priority of the predetermined sources for access to the channel, and a plurality of selection circuits, for each of the plurality of channels, for receiving input signals from at least one of the predetermined sources and the source identification information of the predetermined sources from the plurality of storage units, each of the election circuits selecting one of the plurality of inputs in response to the source identification information, as claimed in claims 37-50. In addition, Baker, *et al.* fails to teach or suggest a method of transferring a signal to a channel which includes storing source identification information for a plurality of predetermined sources, the source identification information indicating an order of priority of the plurality of predetermined sources for access to the channel, and providing a plurality of selection circuits for receiving input signals from at least one of the plurality of predetermined sources and the source identification information of the plurality of predetermined sources, each of the selection circuits selecting one of the plurality of input signals in response to the source identification information, as claimed in claims 51-72.

In the present invention as claimed, a storage unit is dedicated to a single channel and stores source identification information for a plurality of predetermined sources which indicate the order of priority of the plurality of predetermined sources. A plurality of selection circuits receive the source identification information from the storage unit, and, in response to the source identification information, select one of a plurality of input signals from the plurality of predetermined sources. In contrast, Baker, *et al.* discloses receiving an input packet and determining a channel number for that input packet.

In Baker, *et al.*, a single input signal 106 is received and the header information 108 of the input signal 106 is used to determine a channel number for the incoming data packet 106. There is no teaching or suggestion in Baker, *et al.* that the header information 108 indicates an order of priority of a plurality of predetermined sources for access to the channel.

In addition, in Baker, *et al.*, the GRF 80 is not dedicated to a channel and does not store source identification information for a plurality of predetermined sources indicating an order of priority of the plurality of sources for access to the channel.

In addition, the header information 108 in Baker, *et al.* is part of the input signal and is not received from a storage unit.

In addition, the header compare registers and logic 110 of Baker, *et al.* do not select one of a plurality of input signals, as only one input signal is received. Rather, in Baker, *et al.*, the two field select registers 122 and 126 specify the bit fields in WD0 and WD1 of the incoming packet 106 that will be matched to an expected value by the comparator logic and the two compare value registers 120 and 124 specify the expected bit patterns that will be matched against the selected bit fields in WD0 and WD1 of the incoming packet 106.

Baker, *et al.* fails to teach or suggest certain elements of the invention set forth in claims 1-22, 23-36, 37-50 and 51-72, as discussed above. Therefore, it is believed that the amended claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-4, 8-54 and 58-72 under 35 U.S.C. 102(e) as being anticipated by Baker, *et al.*, and the rejections of claims 5-7 and 55-57 under 35 U.S.C. § 103(a) based on Baker, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

In connection with this matter, please charge any otherwise unpaid fees which may be due or credit any overpayment to Deposit Account No. 501798.

Respectfully submitted,

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